

Compal Confidential

Intel M/B Schematics Document

Kabylake-U(2+2)-DDR4 SODIMMx2 (1.2mm_6L)

~~nVidia N16 gDDR5-2GB~~

~~(N16S-6TR GM108-679/779 GeForce MX130)~~

~~(N16U-6UR GM108-625/725 GeForce MX110)~~

Date :2018-01-08

Version :v0.3

Project :20180PP_Harry Potter(15.6")

EPK50 :LA-G07DP

(EPK52 :LA-G07EP=>v0.2 for PV)

~~(EPK50 :KBLU_2G:LA-G07AP)~~

~~(EPK52 :KBLR_2G:LA-G07BP)~~

~~(EPK52 :KBLR_2G:LA-G07CP)~~

(EPK50 :KBLU:LA-G07DP)

(EPK52 :KBLR:LA-G07EP)

DIS

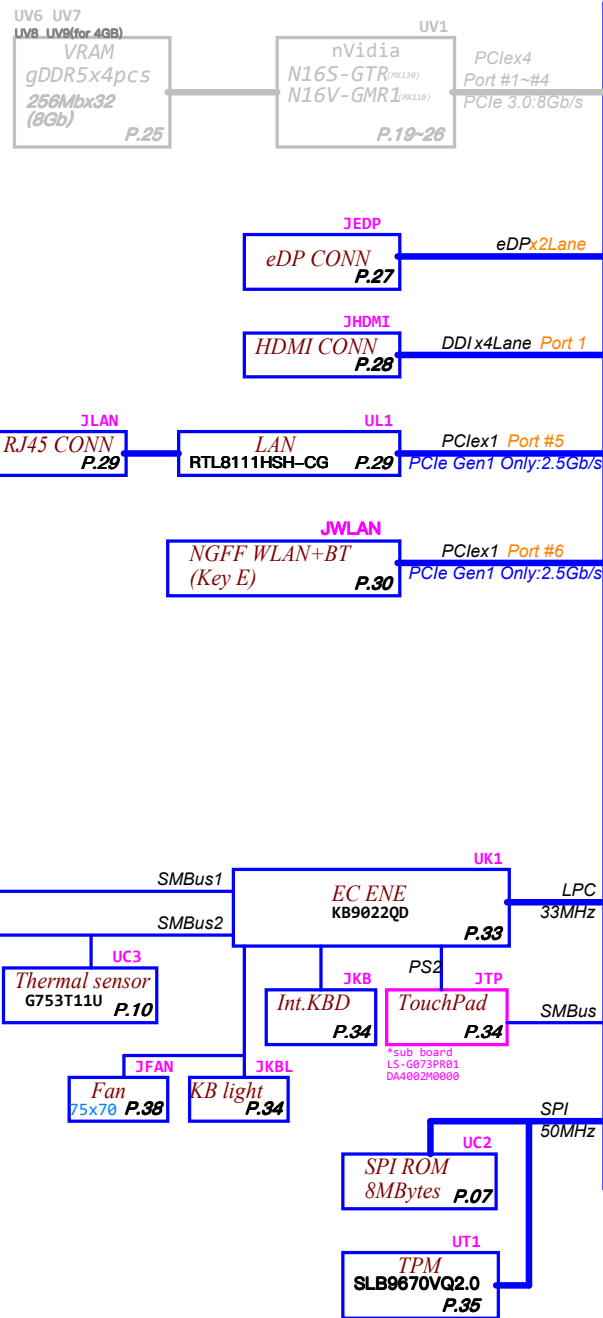
UMA

(Modified&Ref from: 01. "NFLC_KBLR_LAE802PR10_MV_FINAL")

(02. "Canadiens_LA-F035P-R10_KBL-UR_2017-06-23_CPU")

(02. "CNL-U ORB_DDX02_LA-F152PR01_0822B")

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				Date	Monday, January 08, 2018
				Sheet	1 of 59
				Rev	v0.3



Kaby Lake-RU42

1356P BGA

UC1

CHA:JDIMM1(REV)
CHB:JDIMM2(STD)

DDR4-SO-DIMM X 2

P.17~18

Dual Channel Interleaved
DDR4 2133MHz 1.2V

SATA 3.0 Port 0 JHDD P.30

2.5" SATA HDD
(sub board)
*sub board
LS-G072P
DA4002LZ000

SATA 3.0 Port 1 JODD P.30

M.2 SATA SSD
(sub board)
*sub board
LS-G074P
DA6001WR005

PCIe 3.0: 8Gb/s PCIe x2 JSSD P.19

eMMC
(sub board)
*sub board
LS-G075P
DA6001WS005

SATA 3.0 Port 2

USB3.0
5Gb/s

USB2.0 Port 1 JUSB1 P.30

USB3.0 port
(sub board)

USB2.0 Port 2 JUSB2 P.31

USB3.0 port
(sub board)

USB2.0 Port 3 JIIO P.31

USB2.0 Port
(sub board)

Card Reader JEDP P.29

AK6485RB63-GLF-GR
(sub board)
*sub board
LS-G071PR01
DA6001W3000

Camera JEDP P.27

Bluetooth JWLAN P.30

Touch Screen JEDP P.27

HDA 24MHz UA1 JSPK P.32

Internal SPK
(sub board)

HDA Audio codec JHP P.32

Combo Jack
(sub board)

SPI ROM UC2 P.07

TPM UT1 P.35

MB Board Information:
01.DA6001W3000, PCB 29L LS-G071P REV0 I0B(4350M832L01)
02.DA4002LZ000, PCB 29L LS-G072P REV0 HDDB(4350M932L01)
03.DA4002M0000, PCB 29L LS-G073P REV0 TOUCH PADB(4350MA32L01)
04.DA6001W0000, PCB 29M LA-G074P REV0 MB 3(KBLU_2G)
05.DA8001E1000, PCB 29L LA-G078P REV0 MB 3(KBLR_4G)
06.DA6001W1000, PCB 29L LA-G07CP REV0 MB 3(KBLR_2G)
07.DA6001YA000, PCB 29M LA-G07DP REV0 MB 3(KBLU_UMA)
08.DA6001Y0000, PCB 29L LA-G07EP REV0 MB 3(KBLR_UMA)

Sub Board Information:(EPK52)
01.DA6001W3000, PCB 29L LS-G071P REV0 I0B(4350M832L01)
02.DA4002LZ000, PCB 29L LS-G072P REV0 HDDB(4350M932L01)
03.DA4002M0000, PCB 29L LS-G073P REV0 TOUCH PADB(4350MA32L01)
04.DA6001W0000, PCB 29M LA-G074P REV0 MB 3(KBLU_2G)
05.DA8001E1000, PCB 29L LA-G078P REV0 MB 3(KBLR_4G)
06.DA6001W1000, PCB 29L LA-G07CP REV0 MB 3(KBLR_2G)
07.DA6001YA000, PCB 29M LA-G07DP REV0 MB 3(KBLU_UMA)
08.DA6001Y0000, PCB 29L LA-G07EP REV0 MB 3(KBLR_UMA)

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Date: Monday, January 08, 2018				Rev v0.3

Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

BOM Structure Table (1/2)

Function	Stuff	Un-Stuff
DGPU SKU	PX@	
UMA SKU	UMA@	
TPM	TPM@	

R_I3_7020U_QN96@ UC1	R_I3_8130U_QP8K@ UC1
R_SI_I3_7020U_QN96 Y0 2.3G SA0000A38H0 S IC FJ8067703282620 QN96 Y0 2.3G S IC FJ8067703282620 QN96 Y0 2.3G	R_SI_I3_8130U_QP8K Y0 2.2G SA0000A38H0 S IC FJ8067703282227 QP8K Y0 2.2G
R_I7_8550U_QNBF@ UC1	U_I3_7020U_QNZU@ UC1
R_SI_I7_8550U_QNBF Y0 1.8G SA0000A38H0 S IC FJ8067703281816 QNBF Y0 1.8G	U_I3_7020U_QNZU H0 2.3G SA0000A38H0 S IC FJ8067703281816 QNZU H0 2.3G

SOC SMBUS Address Table

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBCLK	+3V_PRIM	DIMM1	0x50	0xA0	0xA1
SMBDATA		DIMM2	0x52	0xA4	0xA5
		Touch PAD	0x2C	0x58	0x59

I3_7100U_R1@ UC1	I3_7100U_R3@ UC1
I3_7100U SA0000A38H0 S IC FJ8067702739738 SR343 H0 2.4G BGA	I3_7100U SA0000A38J0 S IC FJ8067702739738 SR343 H0 2.4G A32I
U_I5_7200U_SR342@ UC1	I5_7200U_R3@ UC1
U_SI_I5_7200U_SR342 H0 2.5G SA0000A37J0 S IC FJ8067702739739 SR342 H0 2.5G BGA	I5_7200U SA0000A37J0 S IC FJ8067702739739 SR342 H0 2.5G A32I
U_I7_7500U_SR341@ UC1	I7_7500U_R3@ UC1
U_SI_I7_7500U_SR341 H0 2.7G SA0000A34H0 S IC FJ8067702739740 SR341 H0 2.7G BGA	I7_7500U SA0000A34H0 S IC FJ8067702739740 SR341 H0 2.7G A32I
R_I5_8250U_QNEF@ UC1	I5_8250U_R3@ UC1
R_SI_I5_8250U_QNEF Y0 1.6G SA0000A38H0 S IC FJ8067703282221 SR3LA Y0 1.6G PCBGA	I5_8250U SA0000A38H0 S IC FJ8067703282221 SR3LA Y0 1.6G A32I
R_I7_8550U_SR3LC@ UC1	I7_8550U_R3@ UC1
R_SI_I7_8550U_SR3LC Y0 1.8G SA0000A38H0 S IC FJ8067703281816 SR3LC Y0 1.8G PCBGA	I7_8550U SA0000A38H0 S IC FJ8067703281816 SR3LC Y0 1.8G A32I

MX110@ UV1	MX130@ UV1
N16V-GMR1-S-A2 SA0000A38H0 S IC N16V-GMR1-S-A2 BGA 595P	N16S-GTR-S-A2 SA0000A38H0 S IC N16S-GTR-S-A2 BGA 595P GPU
2G Micro@ M2G_R1@ X7674032L01	2G Micro@ M2G_R3@ X7674032L08
4G Micro@ M4G_R1@ X7674032L26	4G Micro@ M4G_R3@ X7674032L28
2G Hynix@ H2G_R1@ X7674032L04	2G Hynix@ H2G_R3@ X7674032L07
4G Hynix@ H4G_R1@ X7674032L25	4G Hynix@ H4G_R3@ X7674032L28
2G Samsung@ S2G_R1@ X7674032L05	2G Samsung@ S2G_R3@ X7674032L08
4G Samsung@ S4G_R1@ X7674032L27	4G Samsung@ S4G_R3@ X7674032L30

DAX KBLU-2G@ DA8001Y8000 PCB 29M LA-G07AP REV0 MB 3	DAX KBLR-2G@ DA8001Y8000 PCB 29L LA-G07CP REV0 MB 3	DAX KBLU-4G@ DA8001Y8000	DAX KBLR-4G@ DA8001Y8000	ZZZ EMC for EE X4E@ SMT EMC FOR EE AG07C EPK52
ZZZ DAZ_U2@ DAZ23T00600	ZZZ DAZ_R2@ DAZ23T00600	ZZZ DAZ_U4@ DAZ23T00600	ZZZ DAZ_R4@ DAZ23T00600	
DAX KBLU-UMA@ DA8001Y8000 PCB 29M LA-G07DP REV0 MB 3	DAX KBLR-UMA@ DA8001Y8000 PCB 29L LA-G07EP REV0 MB 3			

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port 2	+3VS	dGPU	
		Thermal Sensor	0x90
		PCH	

Power State

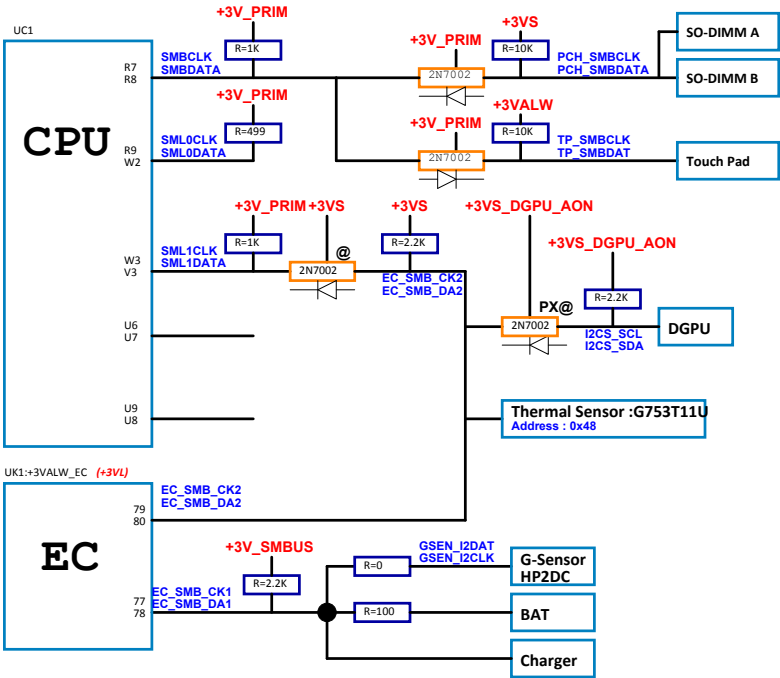
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

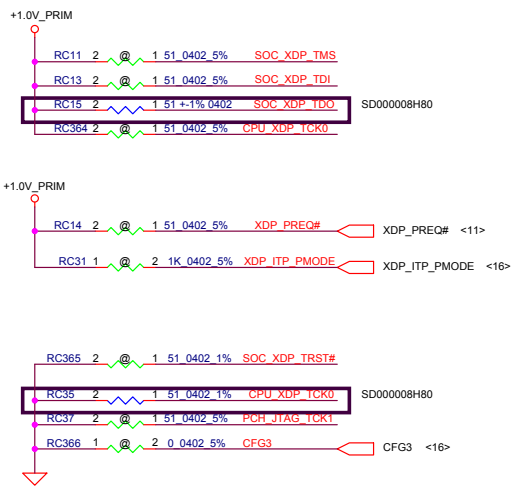
<USB2.0 port>

USB2.0 port	DESTINATION
1	USB3.0 Type-C
2	USB2.0/USB3.0
3	USB2.0/USB3.0
4	BT
5	HD/IR 1/IR 2 Camera
6	IR 2 Camera
7	Card Reader
8	X
9	X
10	X

<PCI-E,SATA,USB3.0/CLK>

Lane#	PCI-E	SATA	USB3.0	DESTINATION	CLK
1			1	USB3.0 Type-C	X
2			2	USB3.0 Type-C	X
3			3	USB2.0/USB3.0	X
4			4	USB2.0/USB3.0	X
5	1		5	GPU(DIS only)	CLK0
6	2		6	GPU(DIS only)	
7	3			GPU(DIS only)	
8	4			GPU(DIS only)	
9	5			LAN	CLK1
10	6			WLAN	CLK2
11	7	0		HDD	X
12	8	1a		ODD	CLK3
13	9			X	X
14	10			X	X
15	11	1b*		NVMe x2	CLK4
16	12	2		SATA SSD	X

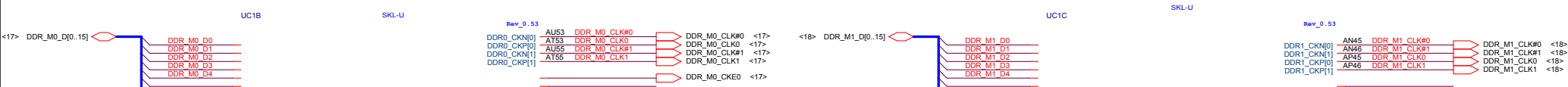




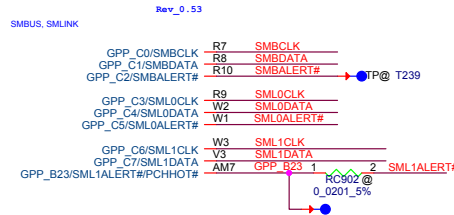
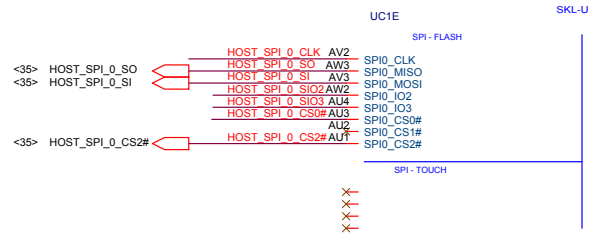
Interleaved Memory

Interleaved Memory

<Cocoa 1020>
PDG#543016, ODT: CPU side no connect, DRAM side connect to VDDQ(Memory down) ; FET+R(SO-DIMM)



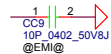
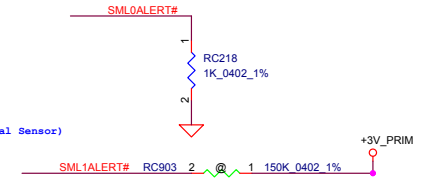
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				LA-G07DP(KBL-U_UMA_6L)	v0.3
				Date: Friday, January 05, 2018	Sheet 6 of 59



SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

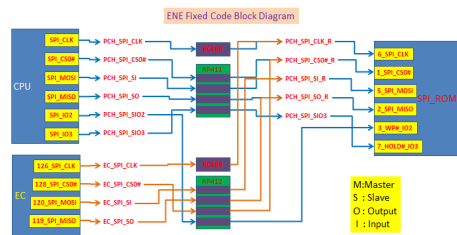
SMB
(Link to XDP, DDR, TP)

SML1
(Link to EC, DGPU, LAN, Thermal Sensor)



Follow 543016_SKL_U_Y_PDG_0_9

RON SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P
MXIC SA00006N100 S IC FL 64M MX25L6473BX21-10G SOP 8P
WINBOND SA000039A30 S IC FL 64M W25Q64FVPSIQ SOIC 8P SPI ROM
Micron SA00005L100 S IC FL 64M N25Q064A13BSCOP SO8W 8P



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				Date	Friday, January 05, 2018
				Sheet	7 of 59

EMI request

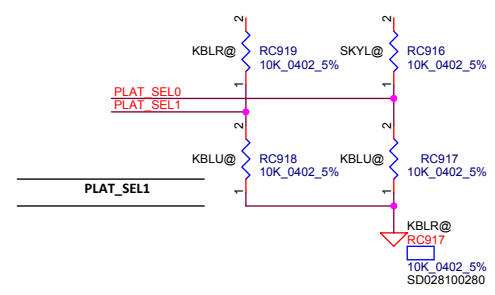
CC183 22P 50V J NPO 0402

UC11

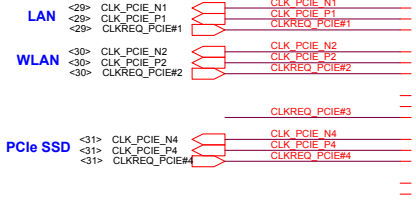
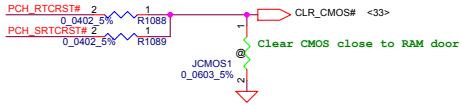
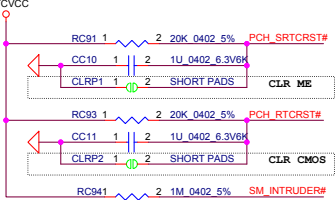
CSI-2

SKL_ULT

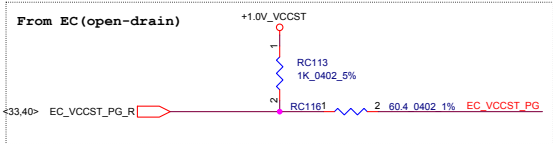
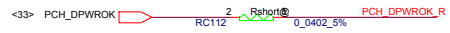
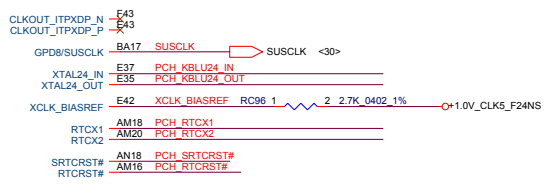
Rev_0.53



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				Date	Friday, January 05, 2018
				Sheet	8 of 59
				Rev	v0.3



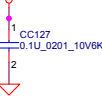
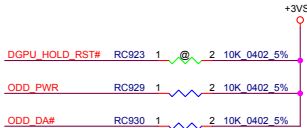
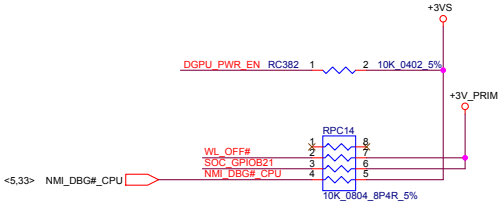
SKL_ULT
CLOCK SIGNALS
Rev_0.53



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Date:				Friday, January 05, 2018				Sheet			
1				9				of			
59				Rev				v0.3			



UC1F
LPSS
SKL-U
ISH
Rev_0.53



<DB> Change Thermal Sensor IC

GSPI0_MOSI (Internal Pull Down):
No Reboot
0 = Disable No Reboot mode. --> AAX05 Use
1 = Enable No Reboot Mode. (PCH will disable the TCO
Timer system reboot feature). This function is useful
when running ITP/XDP.

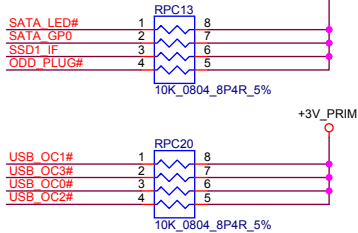
GSPI1_MOSI (Internal Pull Down):
Boot BIOS Strap Bit
0 = SPI Mode --> AAX05 Use
1 = LPC Mode

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				Date:	Friday, January 05, 2018	Sheet	10 of 59

M.2 SSD

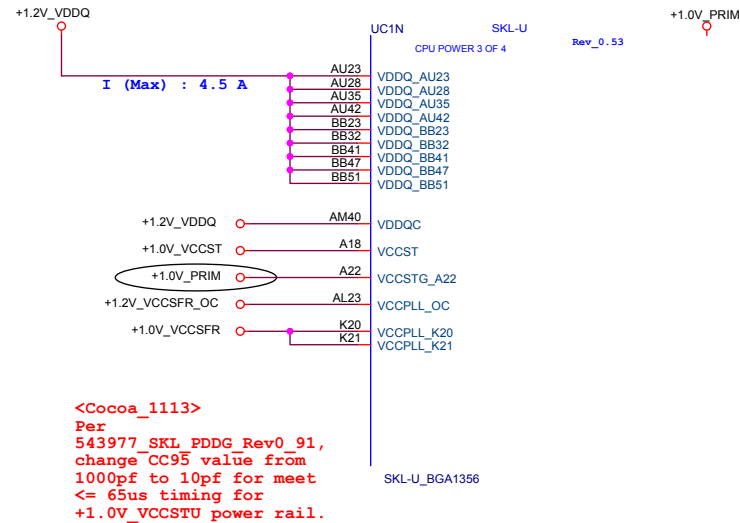
When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

USB_OC2#	N/A
USB_OC3#	N/A
DEVSLP0	N/A
DEVSLP1	N/A
DEVSLP2	NGFF SSD KEY- M
SATA_GP0	N/A
SATA_GP1	ODD_PLUG#
SATA_GP2	PCIE/SATA

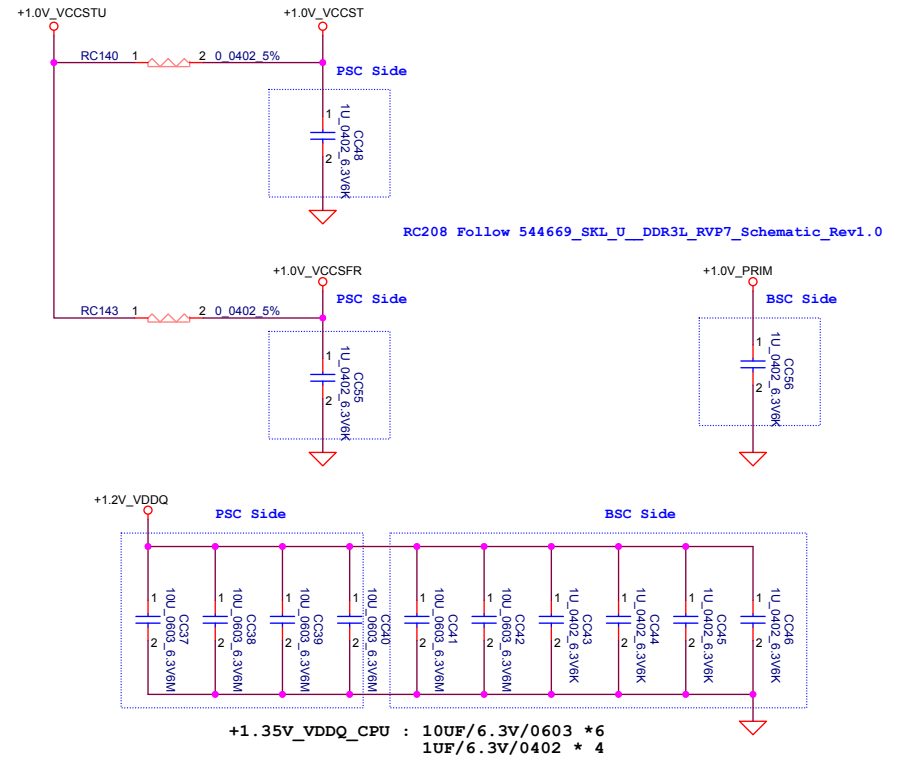
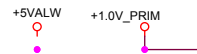


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Issued Date	2017/04/10	Deciphered Date	2019/12/15	Title	SKL-U(7/12)PCIE,USB,SATA
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				Date	Friday, January 05, 2018
				Sheet	11 of 59
				Rev	v0.3

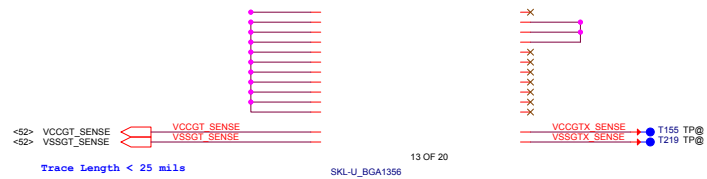
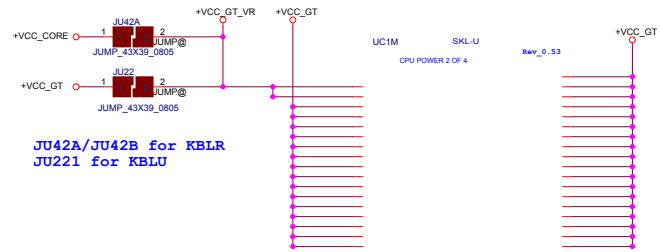
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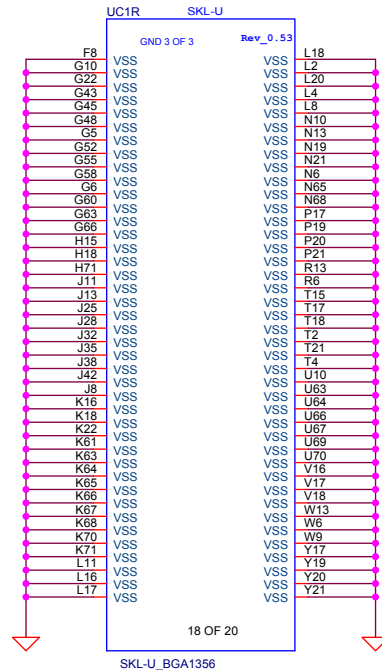
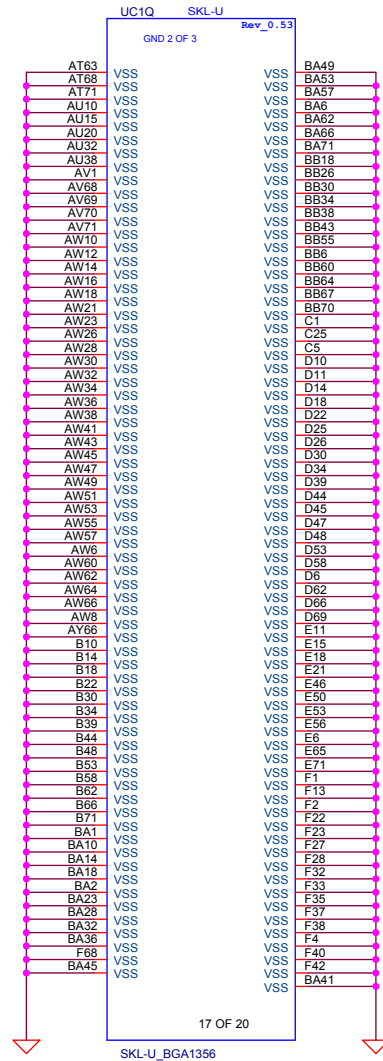
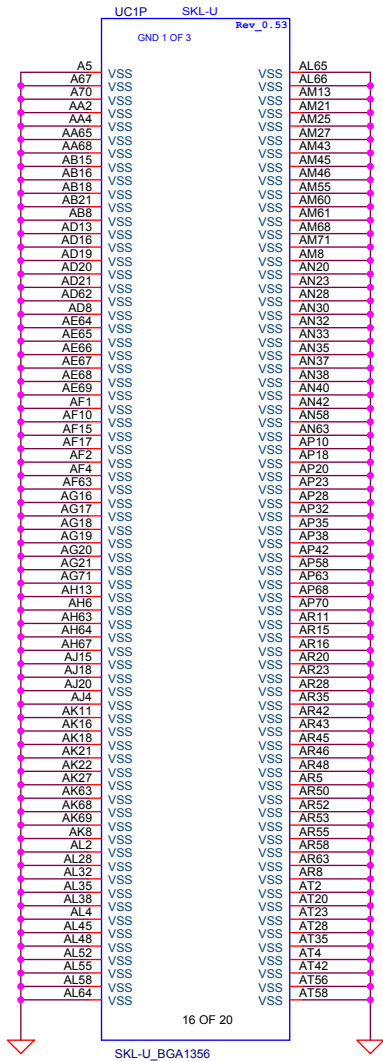
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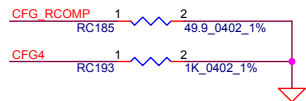
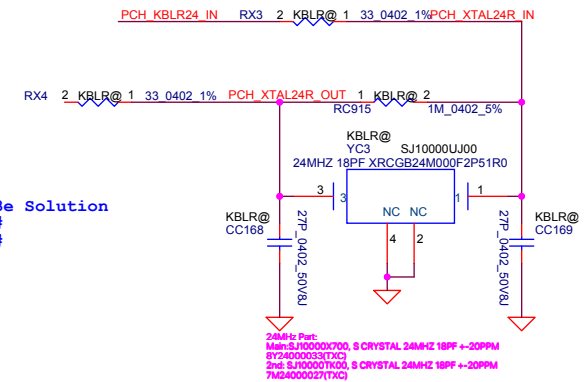
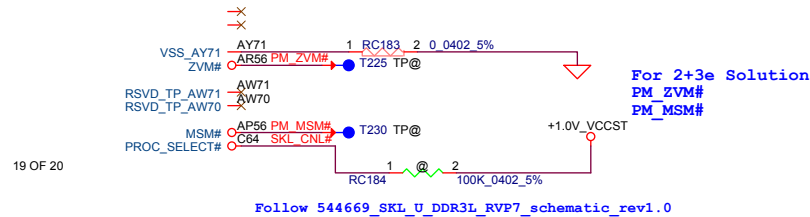
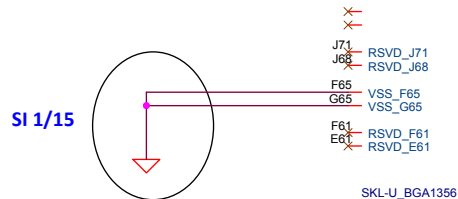
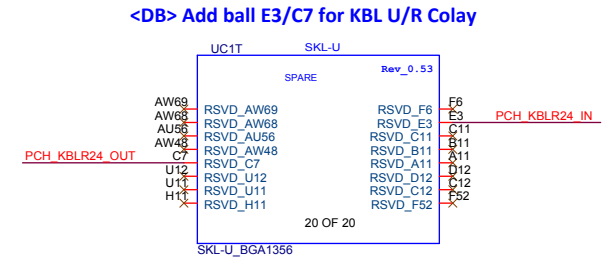
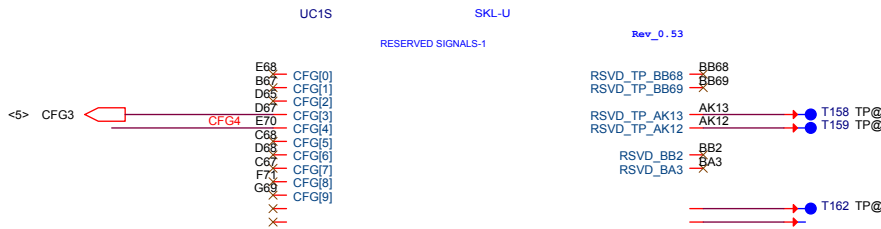
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/04/10	Deciphered Date	2019/12/15	Title	SKL-U(8/12)Power
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				Date	Friday, January 05, 2018
				Sheet	12 of 59
				Rev	v0.3



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			Date: Friday, January 05, 2018	15PM
			14	56



Security Classification		Compal Secret Data		Title	
Issued Date	2017/04/10	Deciphered Date	2019/12/15	Compal Electronics, Inc.	
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				LA-G07DP(KBL-U_UMA_6L)	v0.3
Date: Friday, January 05, 2018				Sheet	15 of 59



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

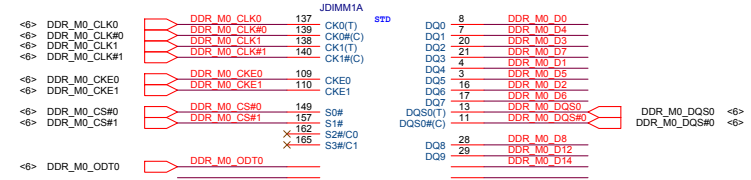
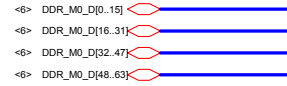
Security Classification		Compal Secret Data		Title	
Issued Date	2017/04/10	Deciphered Date	2019/12/15	SKL-U(12/12)RSVD	
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				LA-G07DP(KBL-U_UMA_6L)	v0.3
Date: Friday, January 05, 2018				Sheet	59

CHANNEL-A

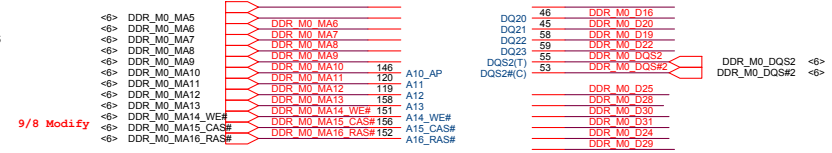
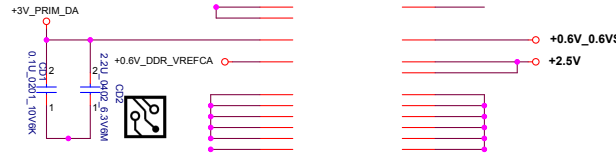
REVERSE TYPE

Interleaved Memory

TOP: JDIMM1 CONN Non-ECC DIMM

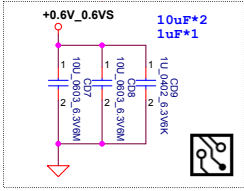
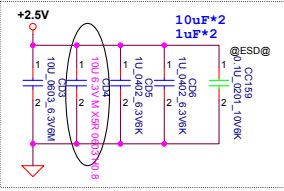


PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

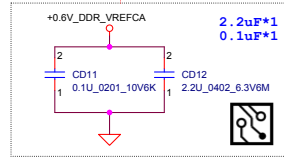


Layout Note:
Place near JDIMM1.257,259

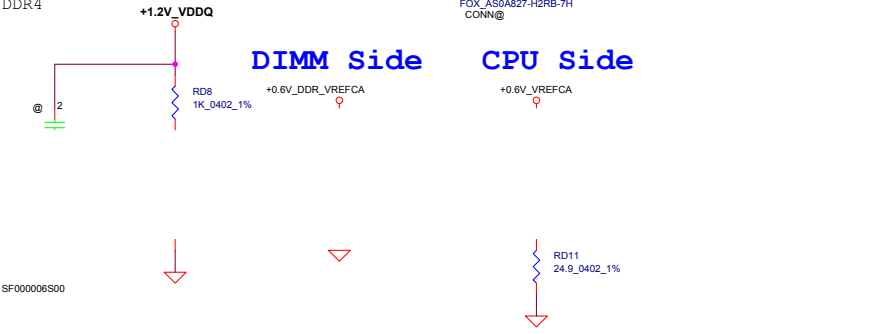
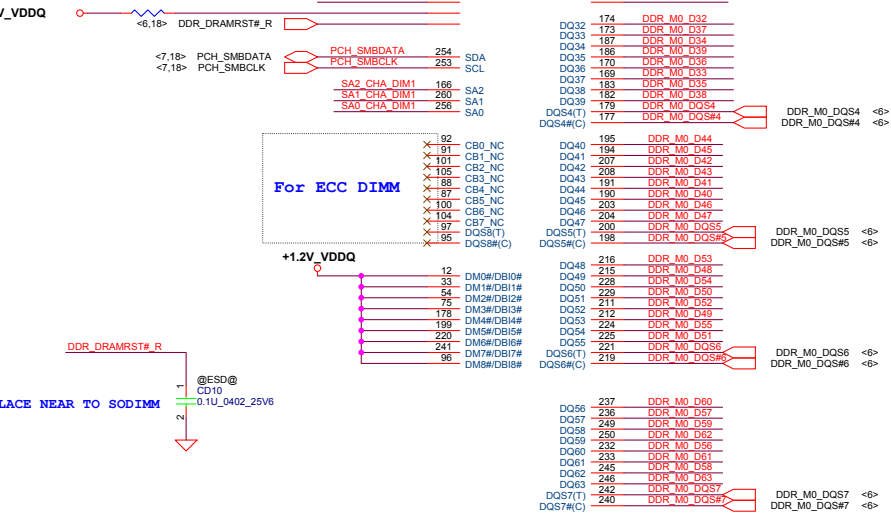
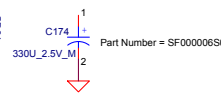
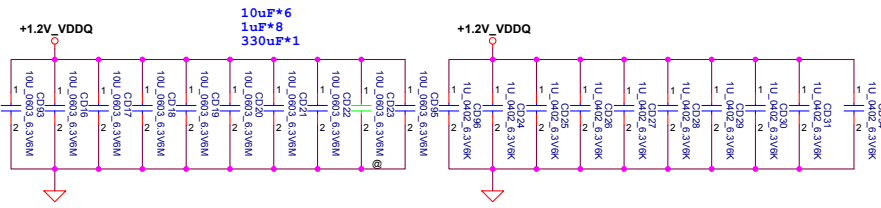
Layout Note:
Place near JDIMM1.258



Layout Note:
PLACE THE CAP near JDIMM1. 164



Layout Note:
Place near JDIMM1



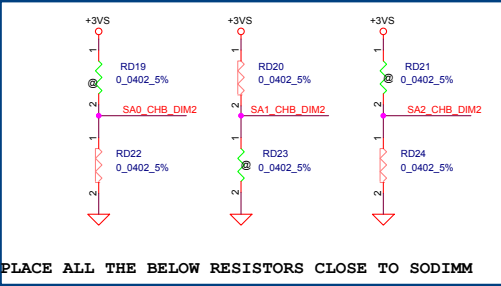
Security Classification	Compal Secret Data		Title	
Issued Date	2017/04/10	Deciphered Date	2019/12/15	Document Number
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Date: Friday, January 05, 2018				Sheet 17 of 59

CHANNEL-B

TOP: JDIMM2 CONN Non-ECC DIMM

Interleaved Memory

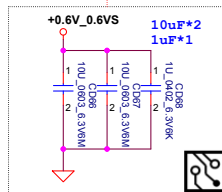
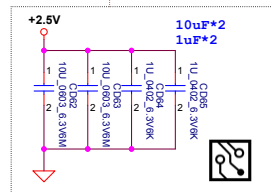
STD (5.2 mm)



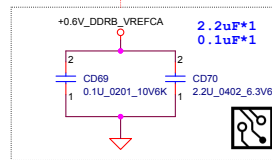
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM2.257,259

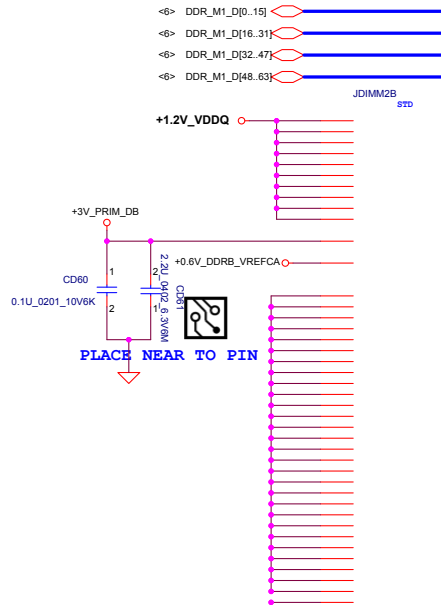
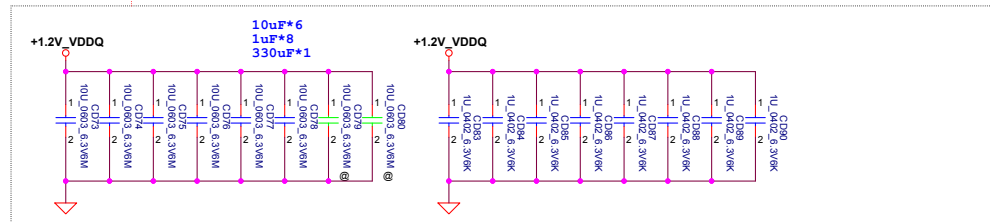
Layout Note:
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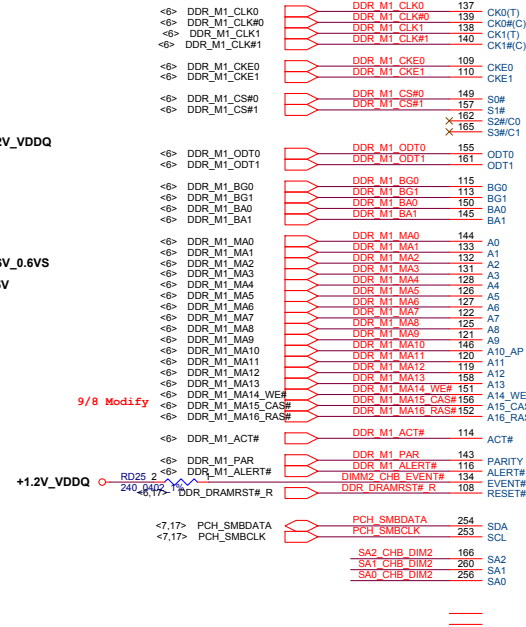
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2



Layout Note:
Place near JDIMM2

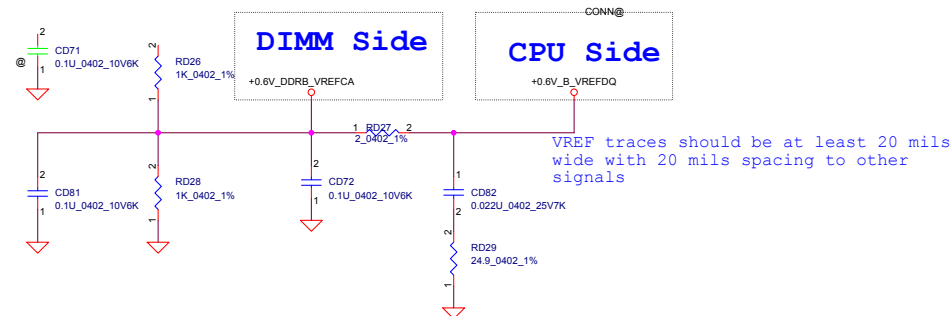


PLACE NEAR TO PIN



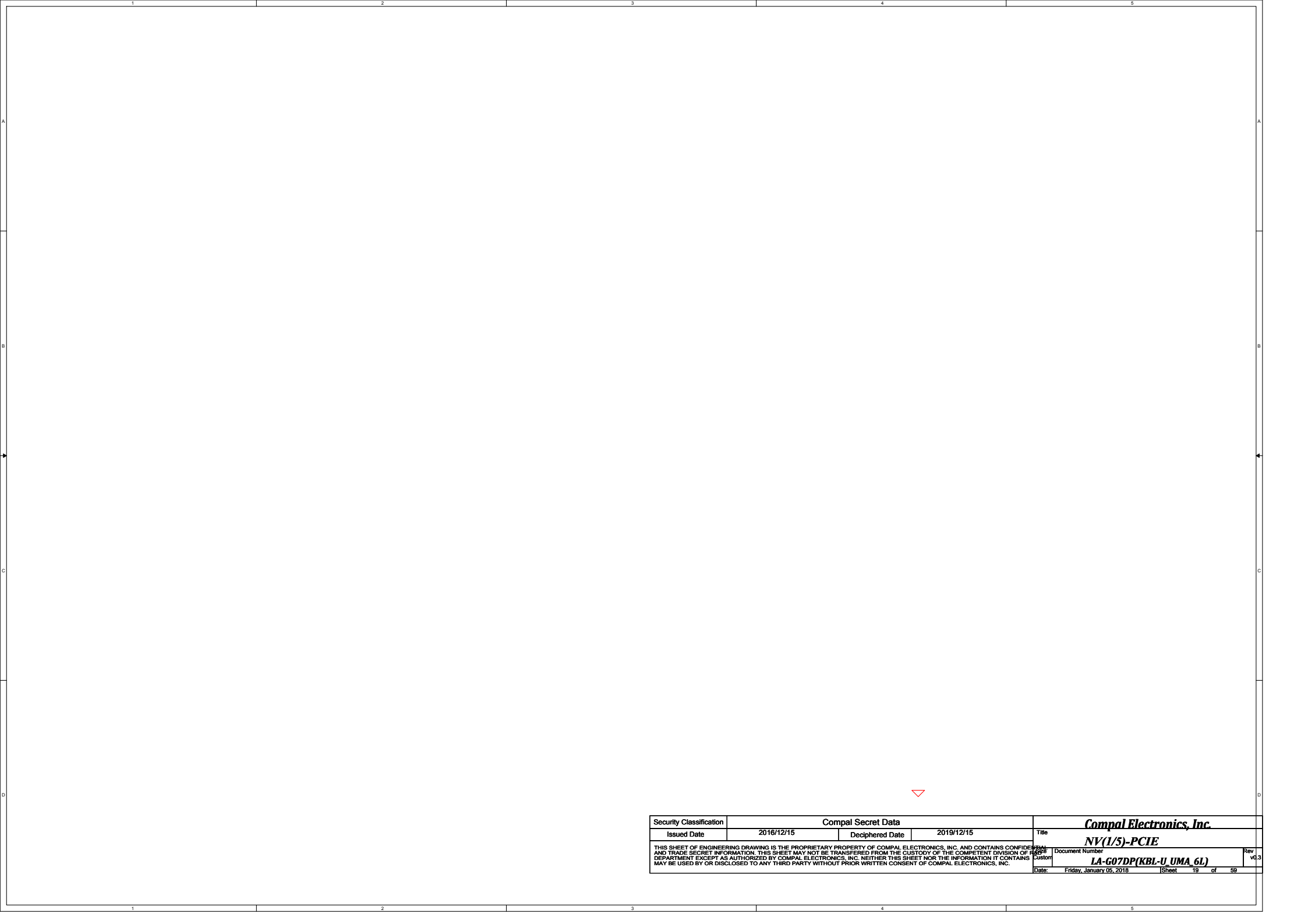
9/8 Modify

+1.2V_VDDQ



VREF traces should be at least 20 mils
wide with 20 mils spacing to other
signals

Security Classification			Compal Secret Data			Compal Electronics, Inc.		
Issued Date			Deciphered Date			Title		
2017/04/10			2019/12/15			P19-DDRIV CHB: DIMM0		
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Date: Friday, January 05, 2018			Sheet			18 of 59		



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2016/12/15	Deciphered Date	2019/12/15	Title	NV(1/5)-PCIE
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				LA-G07DP(KBL-U UMA_6L)	V1.3
				Date: Friday, January 05, 2018	Sheet 19 of 59

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2018/12/15	Deciphered Date	2019/12/15	Title	NV(2/5)-IFP ABCDEF DAC XTAL
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				Rev	V0.3
				Issue	Friday, January 05, 2019
				Sheet	20 of 69

1	2	3	4	5
A				
B				
C				
D				

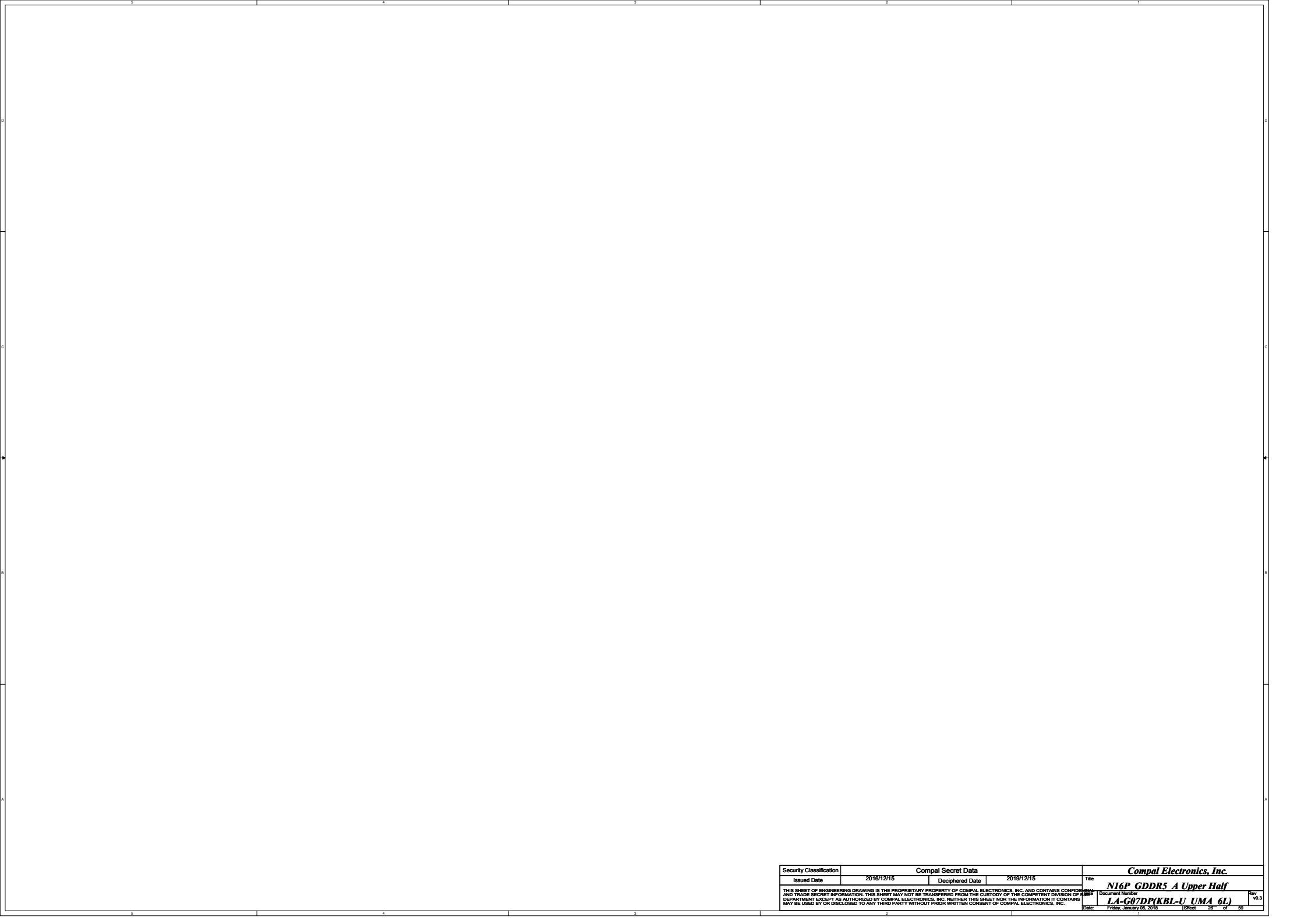
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2016/12/15	Deciphered Date	2019/12/15	Title	NV(3/5)-POWER
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				Rev	v0.3
				Date:	Friday, January 05, 2018
				Sheet	21 of 59

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/12/15	Deciphered Date	2019/12/15	Title
			NV(4/5)-GPIO/Strap	
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			LA-G07DP(KBL-U_UMA_6L)	v0.3
			Date: Friday, January 05, 2018	Sheet 22 of 89

Security Classification		Compal Secret Data		Title	
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2016/12/15		2019/12/15		LA-G07DP(KBL-U, U/MA, 6L)	
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Date: Friday, January 05, 2018				Sheet 23 of 59	

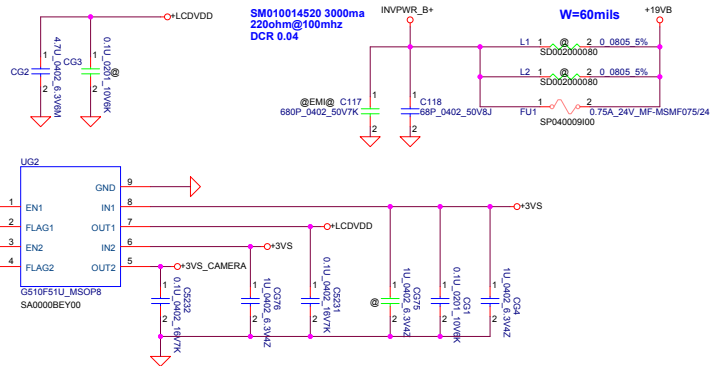
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Issued Date	2016/12/15	Deciphered Date	2019/12/15	DCPU DC/DC Interface
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			Date:	Friday, January 05, 2018
			Sheet	24 of 59

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				Date: Friday, January 05, 2018 Sheet 25 of 59		

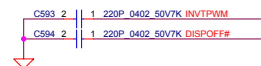
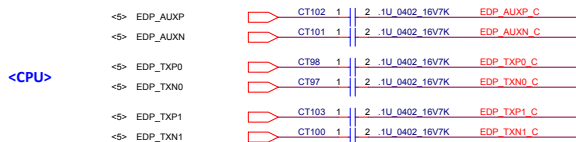
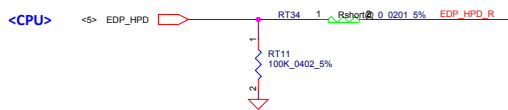
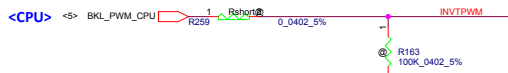
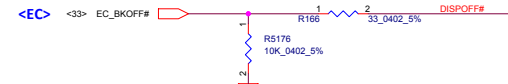
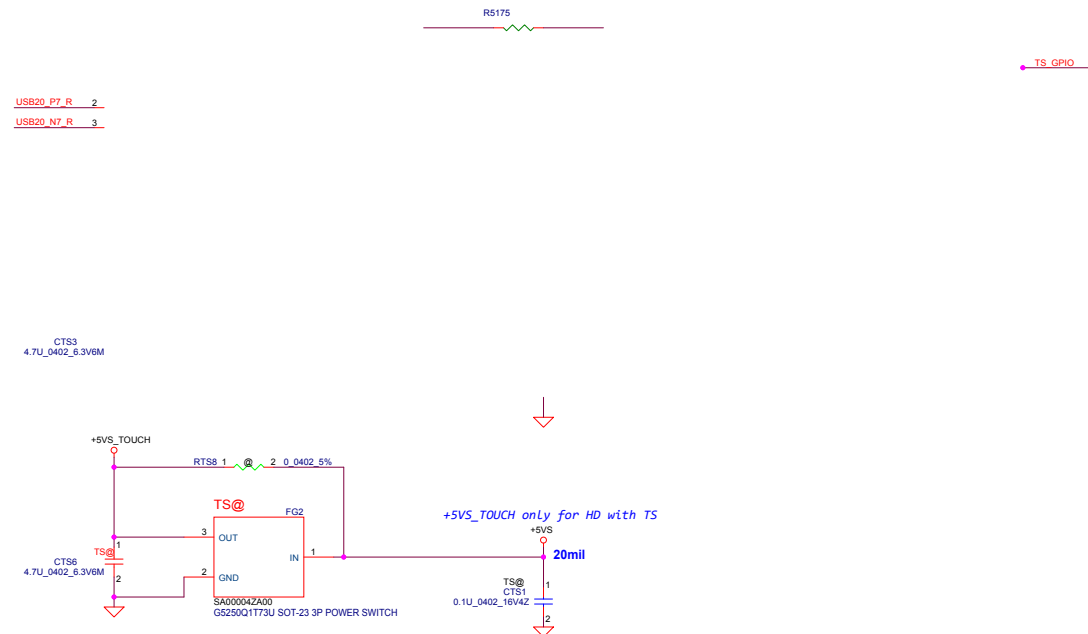
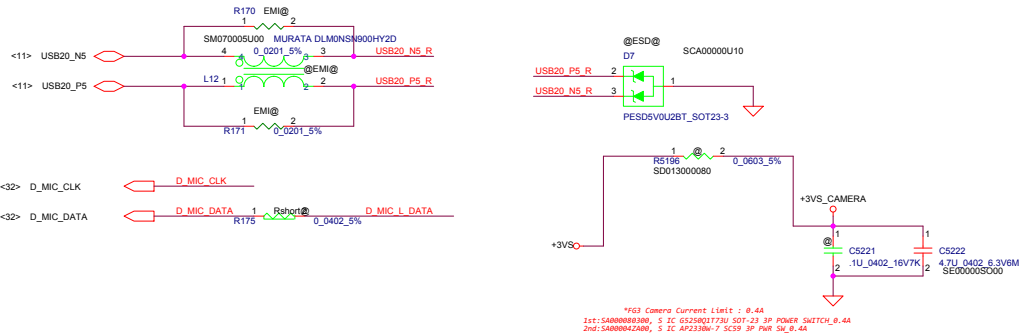


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				Document Number
				LA-G07DP(KBL-U UMA 6L)
				Date
				Friday, January 05, 2018
				Sheet
				25 of 59

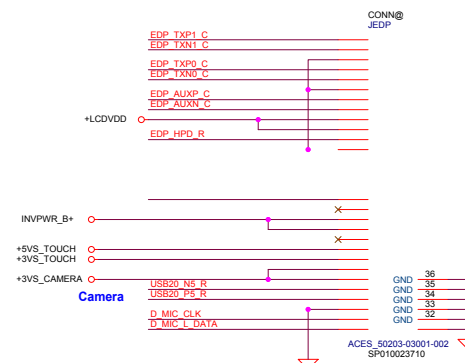
eDP Power



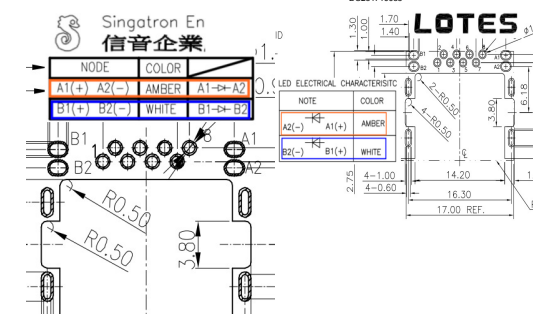
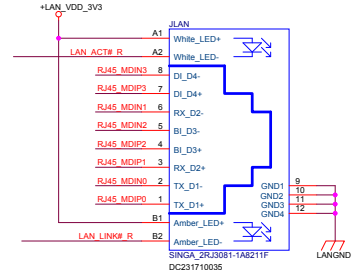
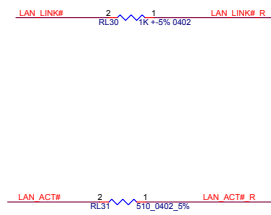
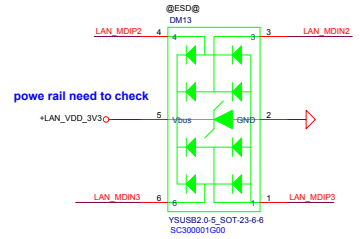
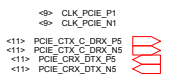
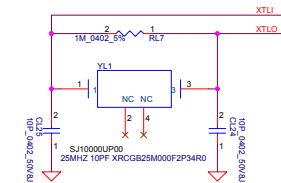
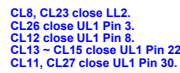
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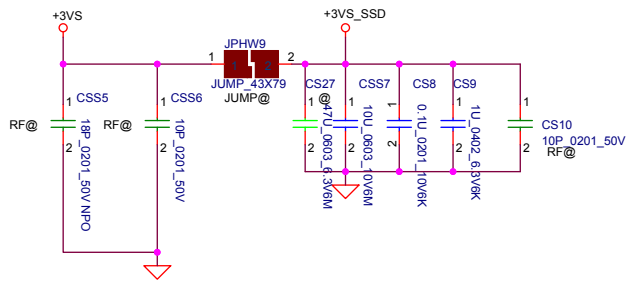
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Date:	Friday, January 05, 2018	Sheet	27	of 59



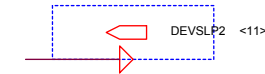
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				Doc#	LA-G07DP(KBL-U_NA_6L)
				Rev	v0.3



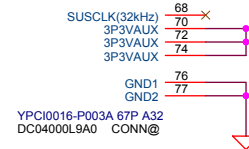
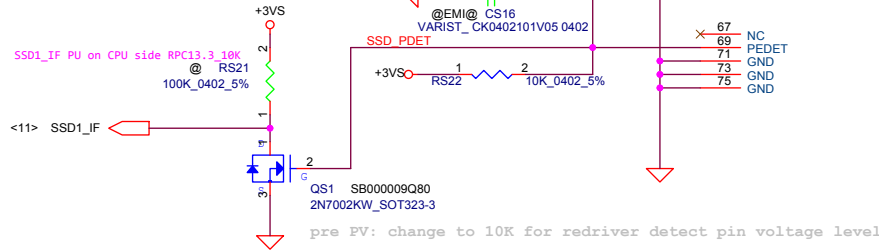
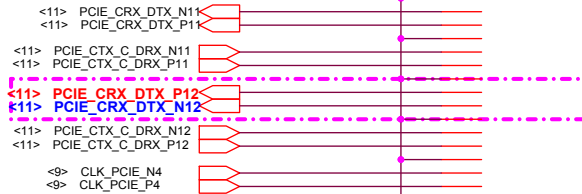
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Figure 12-1. PCI Express® Link Configurations Supported by the Guidelines in this Chapter

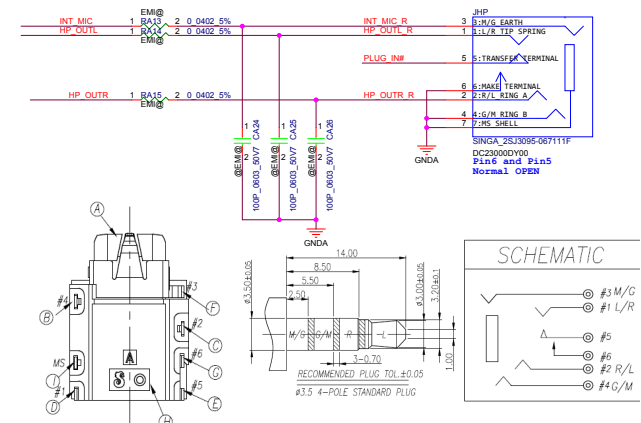
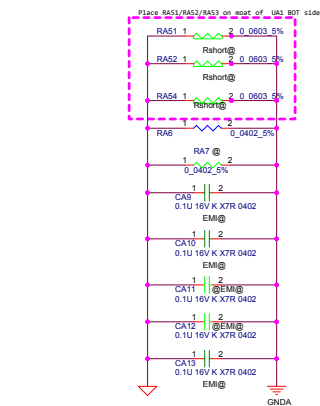
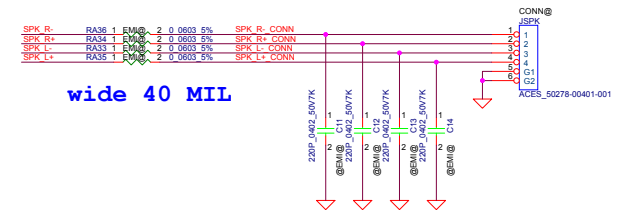
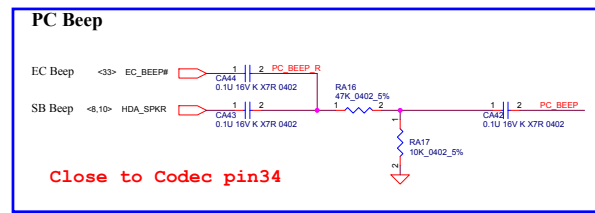
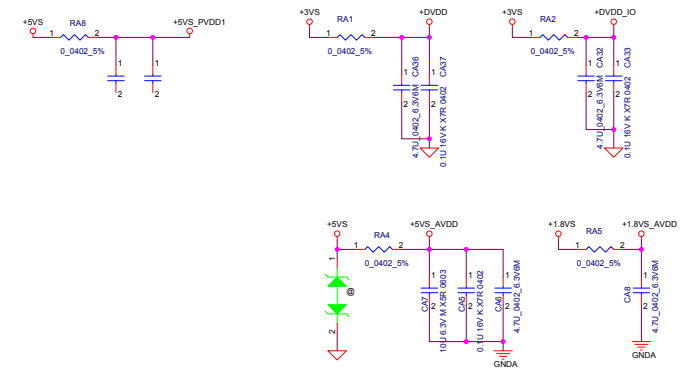
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PCIe® Lane #	1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1			RP 5				RP 9			
	1x4 LR	RP 1			RP 5				RP 9			
	2x2	RP 1	RP 3	RP 4	RP 5				RP 9		RP 11	RP 12
	1x2+2x1	RP 1	RP 3	RP 4	RP 5				RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1	RP 5				RP 9		RP 11	RP 12
Premium-U	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11
	1x4	RP 1			RP 5				RP 9			
	1x4 LR	RP 1			RP 5				RP 9			
	2x2	RP 1	RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12
	1x2+2x1	RP 1	RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1	RP 5	RP 7	RP 5		RP 12	RP 11	RP 9	
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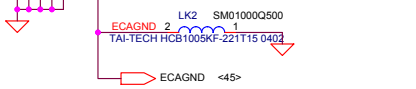
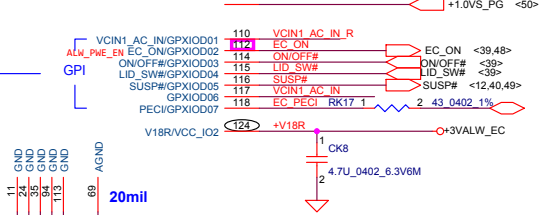
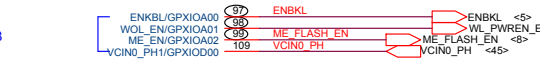
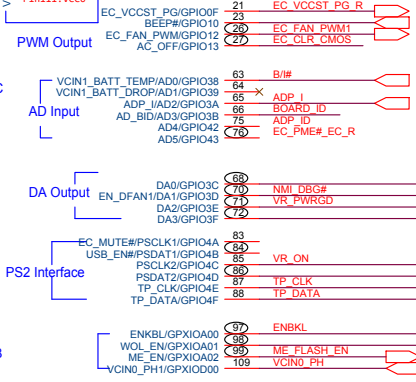
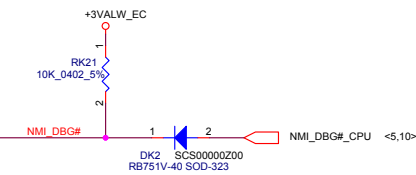
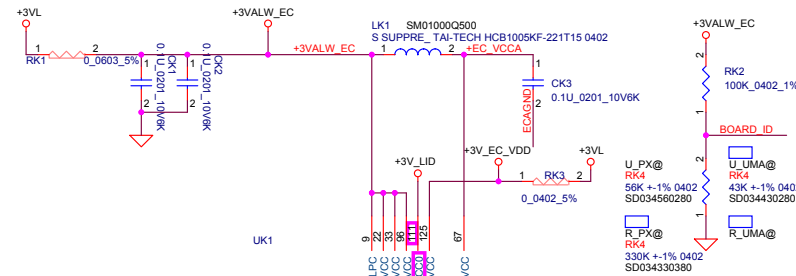
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39	GND	PCIeM/Mo_D09000NU90_MZVLW10HMLH-009H1 F73H1Q 0FH	39	GND	Return Current Path	40	GND	Return Current Path
41	PETR0	PCIe TX	42	N/C		43	TXP	Transmitter Differential Signal Pair
43	PETR1	PCIe TX	44	N/C		45	TXN	Transmitter Differential Signal Pair
45	GND	Return current path	46	N/C		47	RXP	Receiver Differential Signal Pair
47	PERP0	PCIe Rx	48	N/C		49	PERP1	Receiver Differential Signal Pair
49	PERP0	PCIe Rx	50	PERST#		51	GND	Return Current Path
51	GND	Return current path	52	CLKREQ#		53	GND	Return Current Path



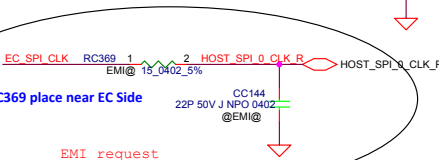
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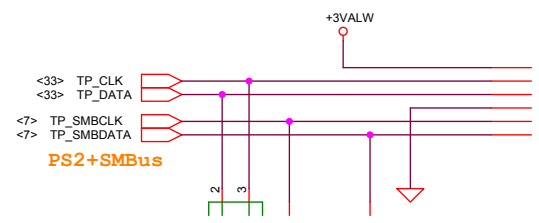
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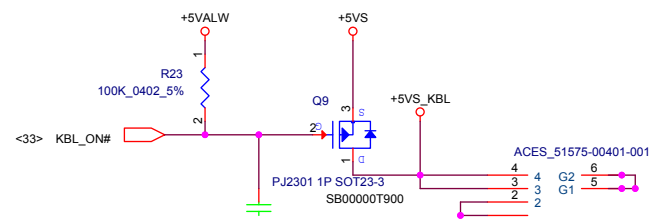


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				Date:	Tuesday, January 09, 2018	Sheet 33 of 59

TP Button BD Connector

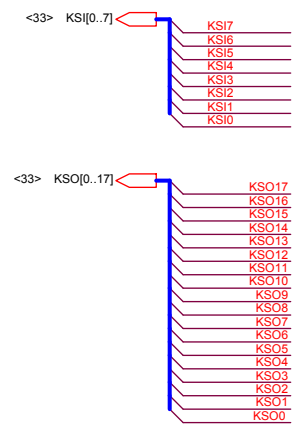


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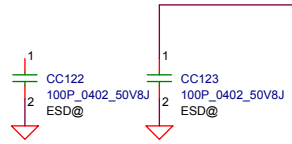
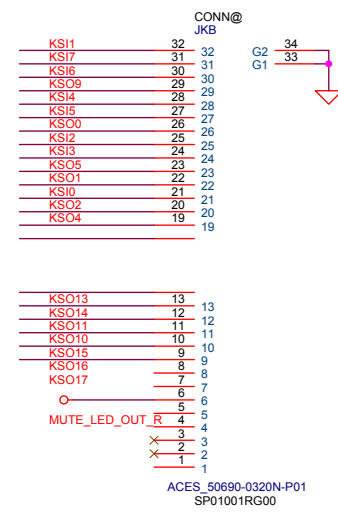


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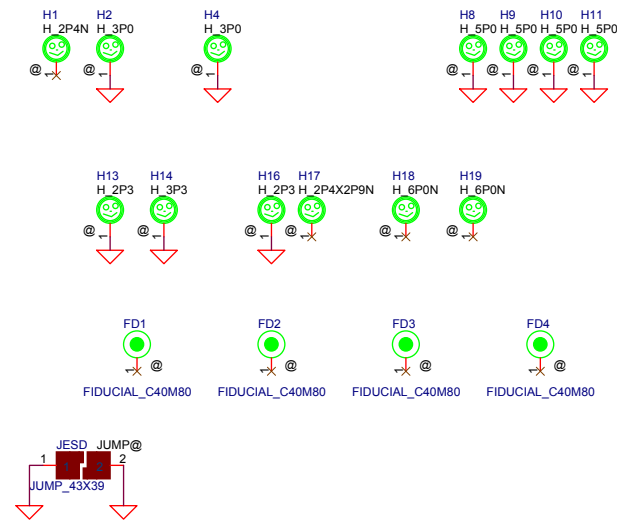
Keyboard conn



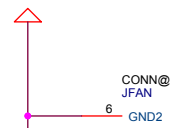
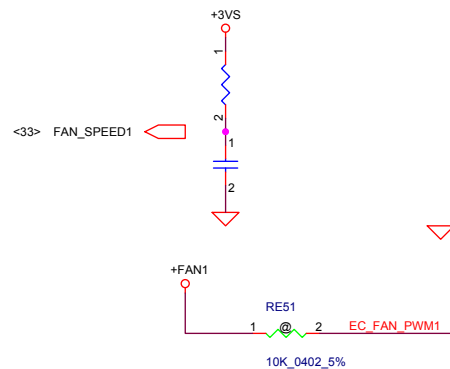
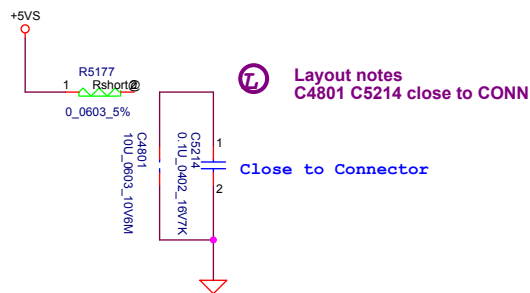
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Pin32	5V	5V



CPU



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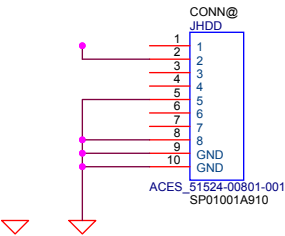
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				Date	Friday, January 05, 2018
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2.5" SATA HDD

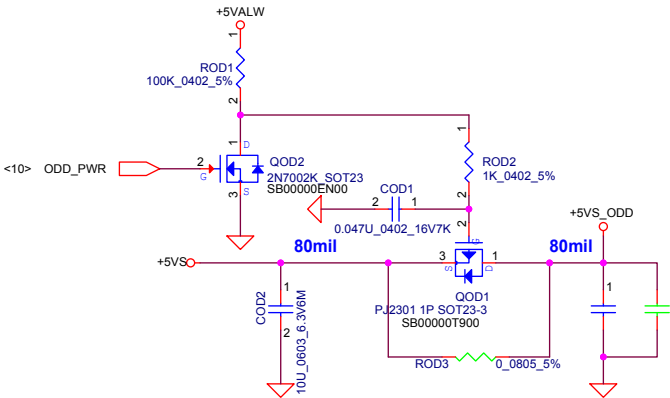
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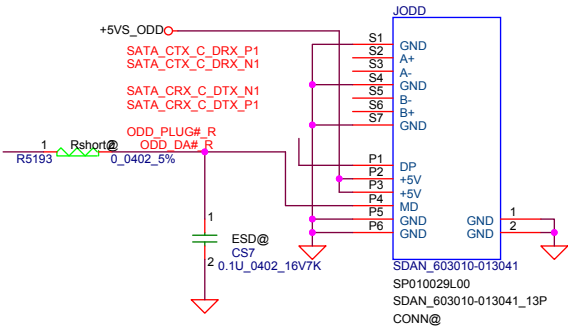
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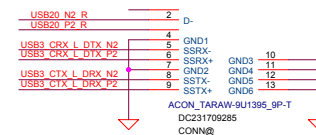
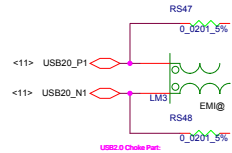
SATA ODD



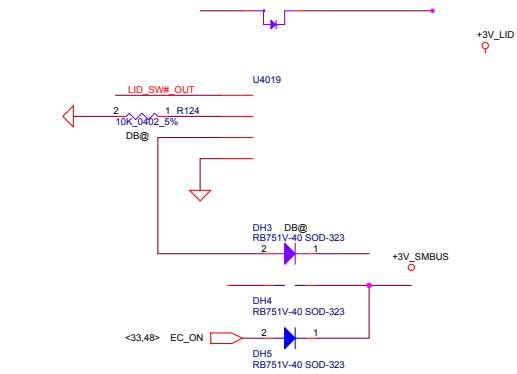
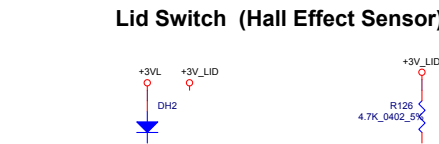
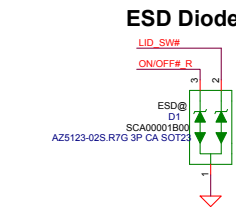
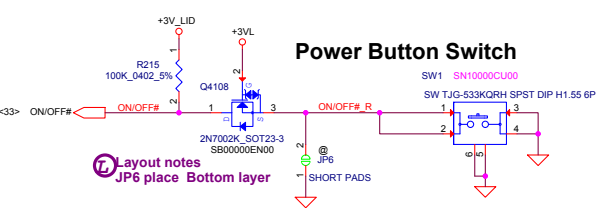
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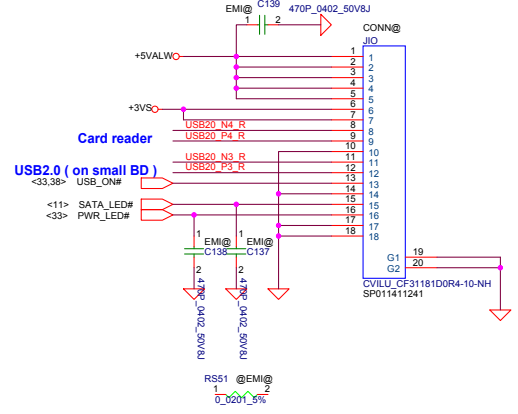
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2018/08/24		2018/08/24		Sheet	
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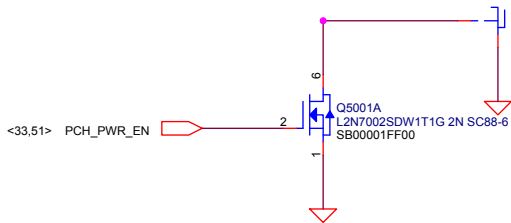
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				Date:	Issue	
				Tuesday, January 09, 2018	Sheet	38 of 59



IO BD Connector (USB2.0,Card reader,HDD & PWR LED)



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Date		Tuesday, January 09, 2018		Rev	
Sheet		39		v0.3	
of		59			



+3VS

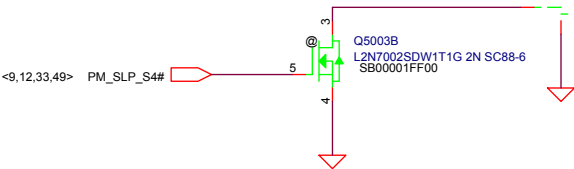
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Date		Friday, January 05, 2018		Sheet	40 of 59

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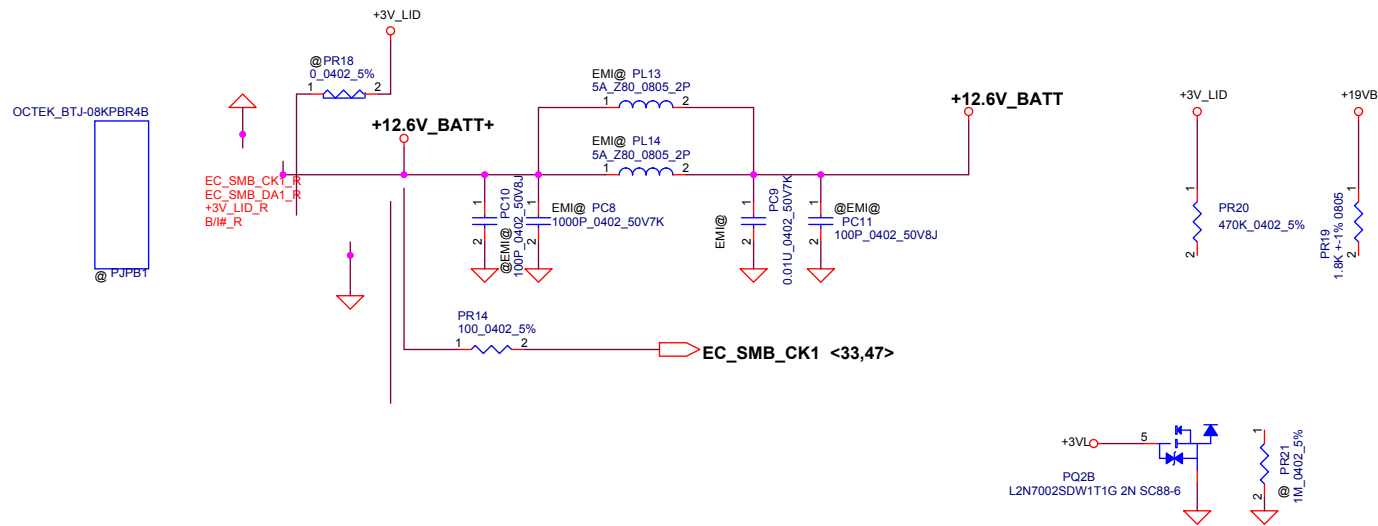
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Date:	Friday, January 05, 2018		Sheet	42	of 59

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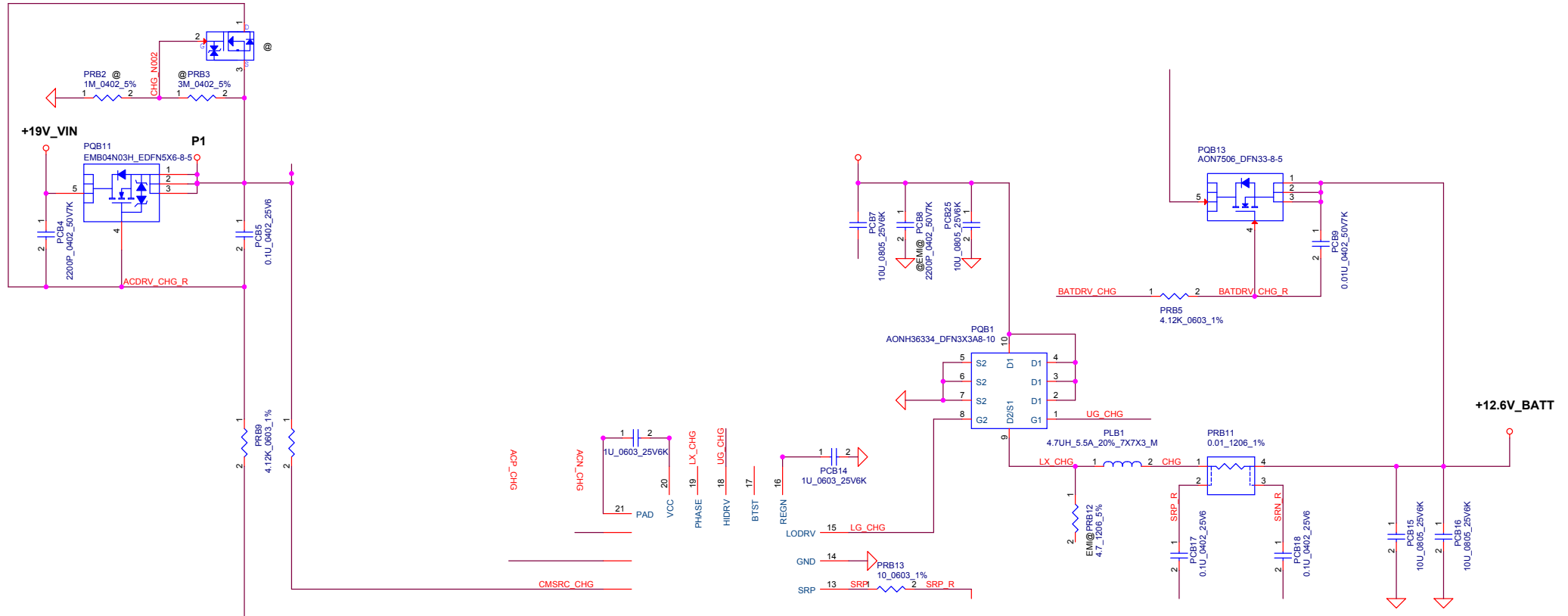
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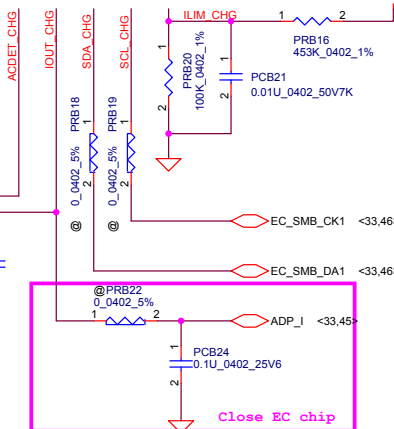


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Title		BATT Conn	
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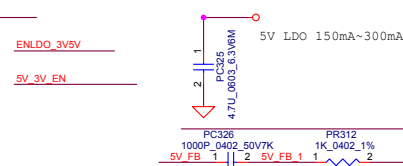
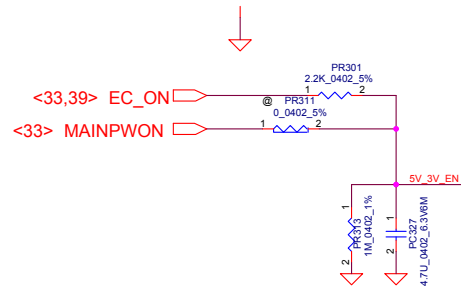
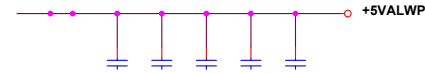
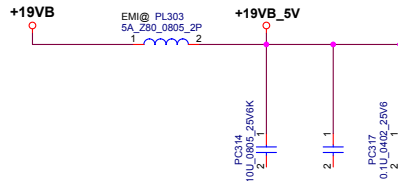
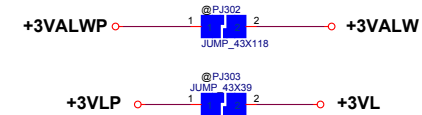
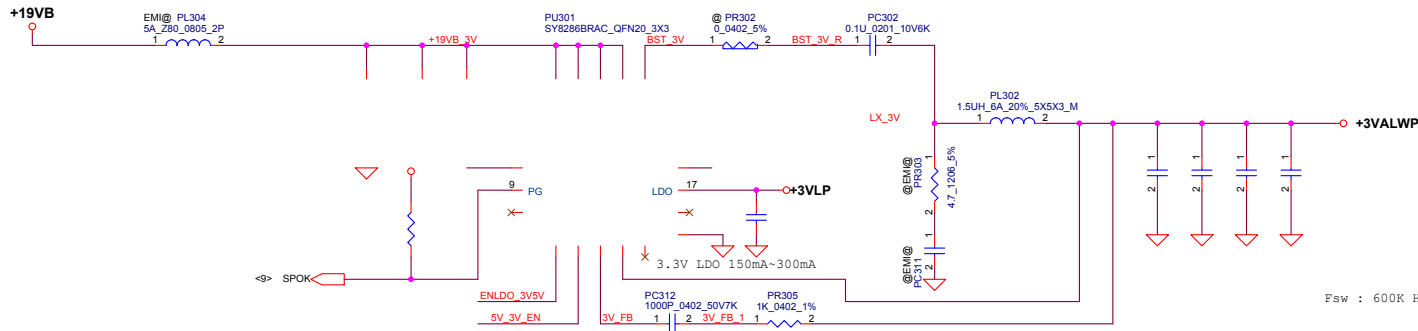
Protection for reverse input



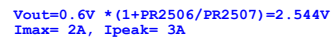
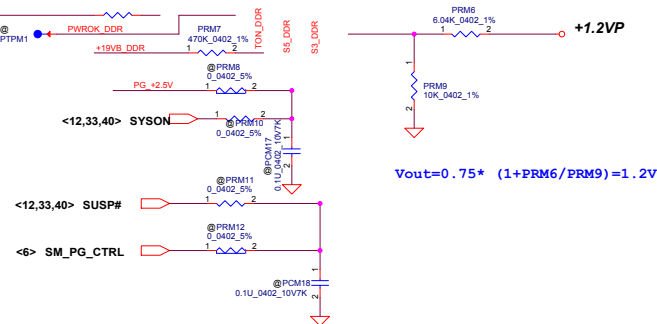
Vin Dectector				
	Min.	Typ	Max.	
L-->H	17.16V	17.63V	18.12V	
H-->L	16.76V	17.22V	17.70V	
VILIM = 20*ILIM*Rsr				
ILIM = 3.3*100/(100+620)/20/0.02				
= 2.291 A				



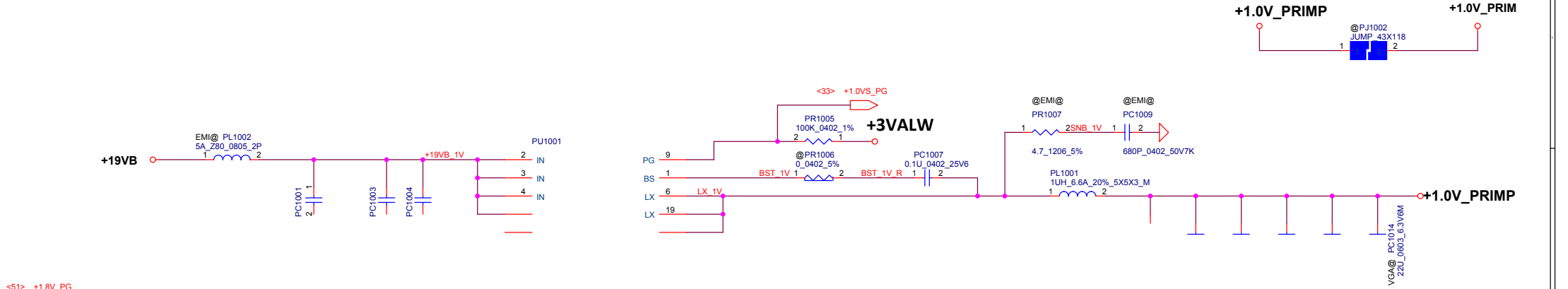
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						Document Number			
						Date:		Friday, January 05, 2018	



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				Date	Friday, January 05, 2018
				Sheet	48 of 59



Security Classification	Compal Secret Data		Title	
Issued Date	2016/09/01	Deciphered Date	2019/09/01	1.2VP/0.6VSP/2.5V
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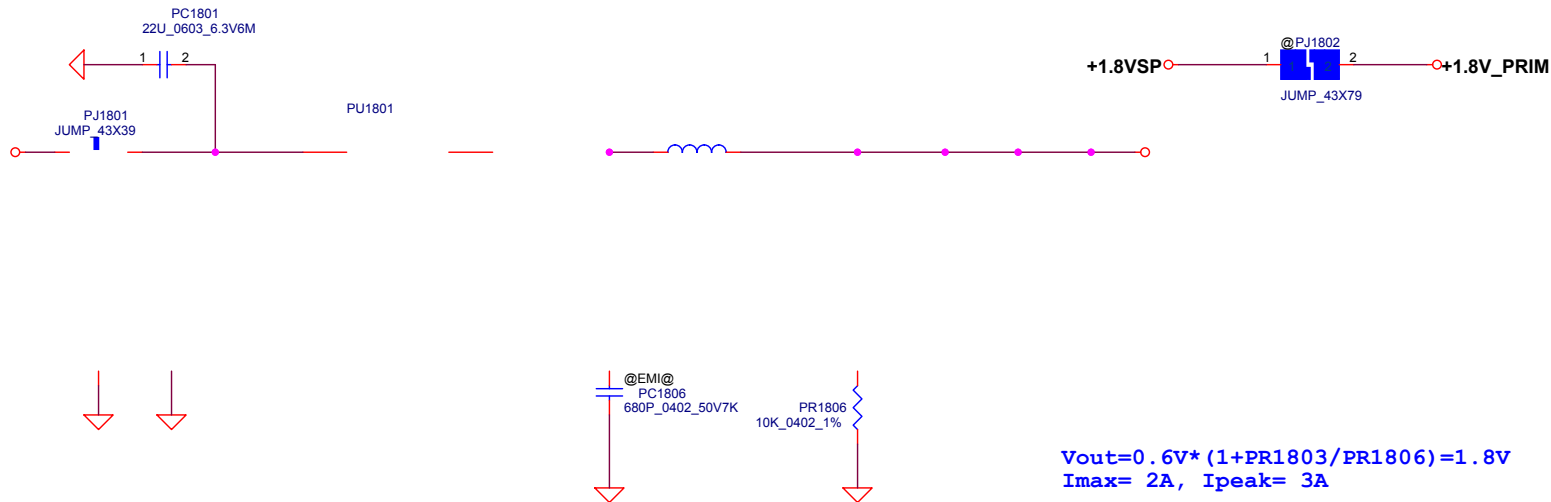


<51> +1.8V_PG

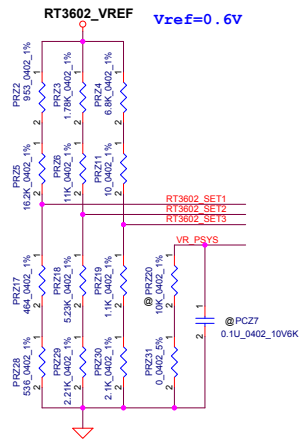
W :H>0.8V ; L<0.4V
W pin don't floating
F have pull down resistor at HW side,
lease delete PR601.

The current limit is set to 6A, 9A or 12A when this pin
is pull low, floating or pull high.

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Issued Date	2016/09/01	Deciphered Date	2019/09/01	1.0V_PRIM		
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				Date:	Friday, January 05, 2018	Sheet 50 of 59

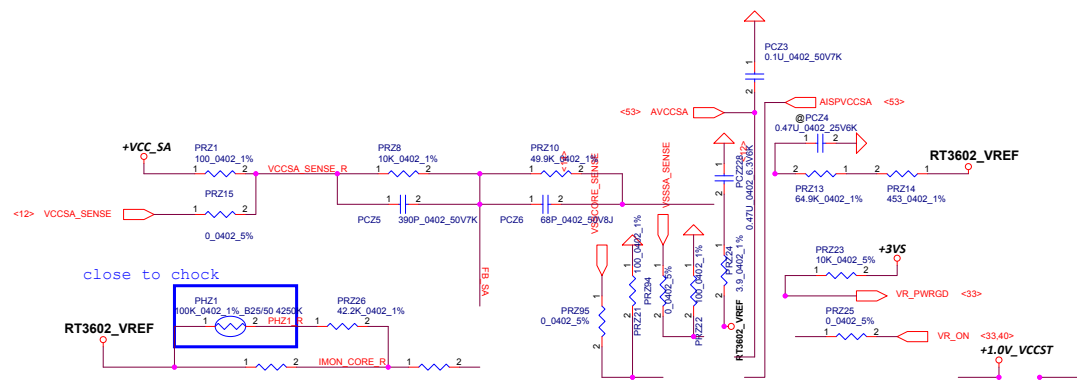
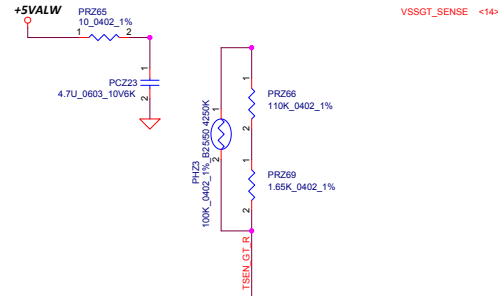
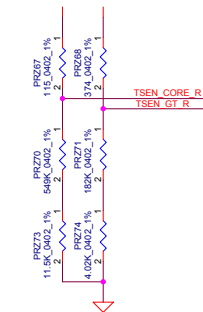


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				Date:	Sheet 51 of 59	

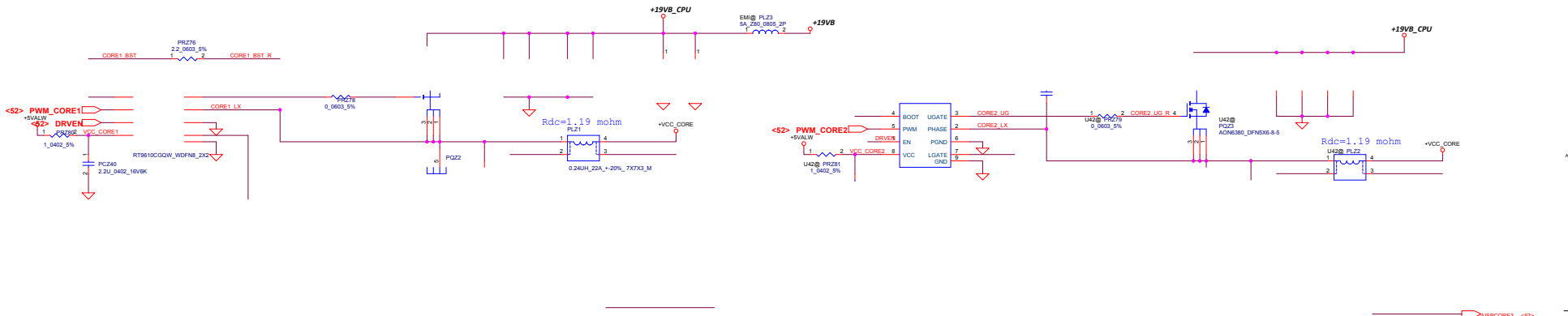


U22
U42

N/A



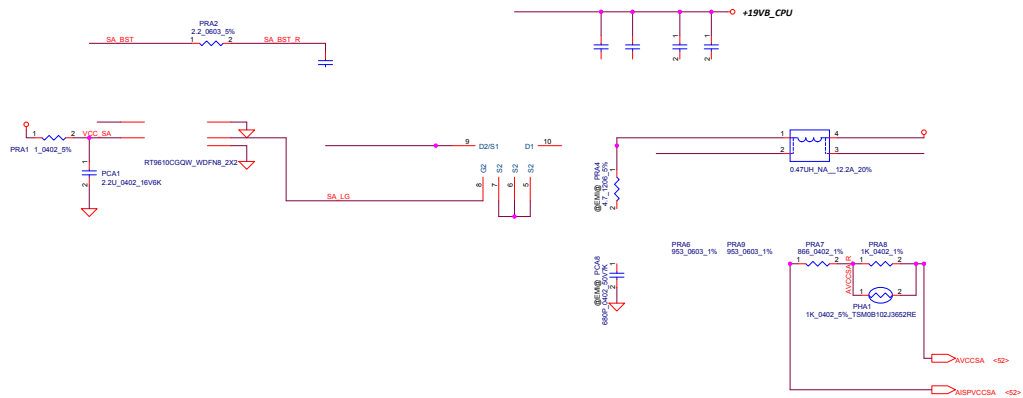
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Issued Date	2016/09/01	Deciphered Date	2019/09/01	Title	CPU_CORE
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Document Number LA-G07DP(KBL-U_UMA_6L)					Date: Friday, January 05, 2018 Sheet 02 of 69



VCC SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

U22
LL=10.3 mohm
TDC=4A
ICCMAX=4.5A
OCP=9.5A

U42
LL=10.3 mohm
TDC=
ICCMAX=5A
OCP=9.5A



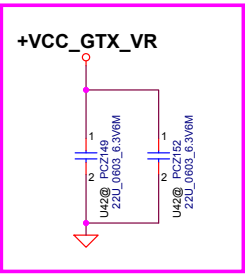
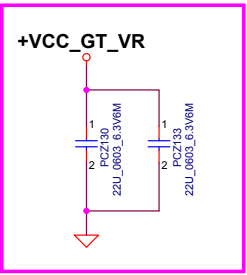
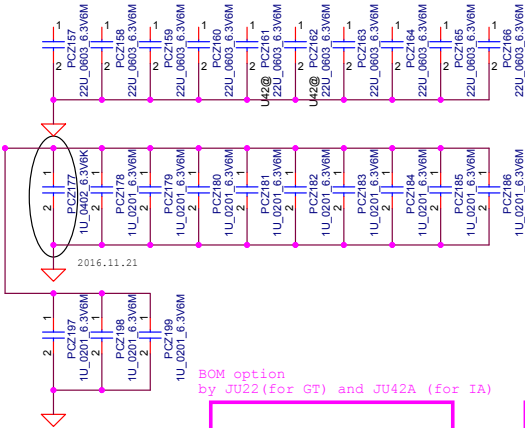
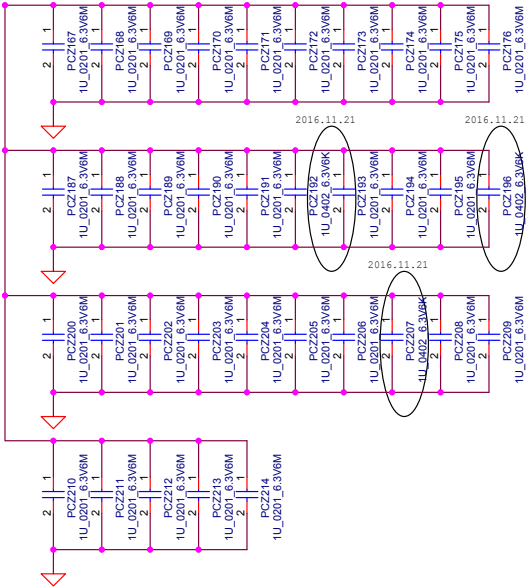
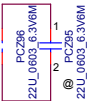
+VCC_CORE

2016.12.29

+VCC_GT

VCC_GT :
U22 & U42
390uF*1
22uF*33
1uF*13

VCC_SA :
U22 & U42
22uF*9
1uF*7



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				Date	Friday, January 05, 2018
				Sheet	54 of 59
				Rev	v0.3

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				LA-G07DP(KBL-U_UMA_6L)	V0.3
				Date: Friday, January 05, 2018	Sheet 55 of 59

Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i>		
Issued Date	2015/09/01	Deciphered Date	2018/09/01	Title		
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Date: Friday, January 05, 2018				Sheet 56 of 59		

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D					D																								
C					C																								
B					B																								
A					A																								
<table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td><td colspan="2">Compal Electronics, Inc.</td></tr><tr><td>Issued Date</td><td>2016/09/01</td><td>Deciphered Date</td><td>2018/09/01</td><td colspan="2">Title</td></tr><tr><td colspan="4" rowspan="2">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td>Size</td><td>Document Number</td></tr><tr><td>Date: Friday, January 05, 2018</td><td>Rev v0.3</td></tr><tr><td colspan="2">Sheet 57 of 59</td><td colspan="3"></td></tr></table>					Security Classification	Compal Secret Data			Compal Electronics, Inc.		Issued Date	2016/09/01	Deciphered Date	2018/09/01	Title		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Date: Friday, January 05, 2018	Rev v0.3	Sheet 57 of 59				
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Sheet 57 of 59																													
5	4	3	2	1																									

